IN THE CLAIMS

1 (Currently Amended). An apparatus, comprising:

a storage device to store data; and

a block to adjust the position of the data in the storage device to account for the sampling rate of the apparatus being different than the rate of the received data. ~~at least one sampling error.~~

2 (Original). The apparatus of claim 1, wherein the block adjusts a portion of the data in response to receiving a plurality of bits in response to sampling a portion of an incoming data.

3 (Original). The apparatus of claim 1, wherein the block comprises a detector to detect the at least one sampling error.

4 (Original). The apparatus of claim 3, comprising a counter block to provide a clock substantially synchronous with the data in response to detecting the at least one sampling error.

5 (Original). The apparatus of claim 1, wherein the block comprises a sampling block to sample incoming data using a plurality of sampling clocks to provide a plurality of samples.

6 (Original). The apparatus of claim 5, wherein the block comprises a multiplexer to receive the plurality of samples and provide a desirable sample to the storage device from the plurality of samples in response to a control signal.

7 (Original). The apparatus of claim 5, including a detector block to adjust the position of the data based on detecting at least one of a phase lag and a phase lead based on the plurality of samples.

8 (Original). The apparatus of claim 1, wherein the block does not shift the data in response to detecting duplicate sampling values of incoming data.

9 (Original). The apparatus of claim 1, wherein the storage device is a variable shift register.

10 (Currently Amended). An apparatus, comprising:

a sampling block to sample incoming data using a plurality of sampling clocks to provide a plurality of samples;

a detector block to detect when the frequency of a sampling clock is different from the rate of the incoming data; and ~~at least one sampling irregularity in the plurality of samples; and~~

a storage device to adjust the position of the data in response to detecting the difference in frequency of the sampling clock and the incoming data. ~~at least one sampling irregularity.~~

11 (Original). The apparatus of claim 10, wherein the storage device is a shift register.

12 (Original). The apparatus of claim 11, wherein the storage device is a variable shift register.

13 (Original). The apparatus of claim 12, further comprising a counter block to count a number of shifts of the variable shift register.

14 (Original). The apparatus of claim 13, further comprising a comma detect block to reset the counter block in response to detecting a unique sequence of bits.

15 (Original). The apparatus of claim 13, wherein the counter block is one of a variable shift register and an adder circuit.

16 (Original). The apparatus of claim 13, wherein the detector is one of a phase detector and an edge detector.

17 (Original). The apparatus of claim 10, wherein the sampling block samples the incoming data using three sampling clocks to provide three samples.

18 (Original). The apparatus of claim 10, further comprising a multiplexer to receive the plurality of samples and provide desirable sample from the plurality of samples to the storage device based on a control signal from the detector block.

19 (Currently Amended). An apparatus, comprising:

a clock block to generate a plurality of sampling clocks;

a sampling block to sample data using the plurality of sampling clocks to generate a plurality of sample values;

a detector block to detect that the frequency of a sampling clock is different from the frequency of the data being sampled; and ~~at least one sample irregularity based on the plurality of sample values; and~~

a shift register to receive at least one of the plurality of sample values and to shift the at least one of the plurality of sample values in response to the difference in frequency between the sample clock and the sampled data. ~~detecting the at least one sample irregularity.~~

20 (Original). The apparatus of claim 19, wherein the detector is an edge detector.

21 (Original). The apparatus of claim 19, wherein the shift register is a variable shift register.

22 (Currently Amended). A method comprising:

storing data in ~~into~~ a storage device; and

adjusting the location of the data in the storage device to account for a difference in the frequency of the sampling rate versus the data rate of the data being received in the storage. ~~synchronization errors.~~

23 (Original). The method of claim 22, further comprising sampling incoming data to provide a plurality of samples.

24 (Original). The method of claim 23, further comprising detecting at least one sampling error in the plurality of samples.

25 (Original). The method of claim 24, further selecting a desirable sample from the plurality of samples and storing the desirable sample in the storage device.

26 (Original). The method of claim 22, wherein sampling the incoming data comprises sampling the incoming data at a rate at least three times faster than the rate of the incoming data.

27 (Original). The method of claim 22, wherein adjusting the location comprises shifting the data by two location in the storage device to account for sampling frequency being slower than a rate of an incoming data.

28 (Original). The apparatus of claim 22, wherein adjusting the location comprises not shifting the data in the storage device to account for sampling frequency being faster than a rate of an incoming data.

Claims 29 and 30 (Canceled).